PATENT ABSTRACTS OF JAPAN

(11)Publication number : 08-168239

(43)Date of publication of application : 25.06.1996

(51)Int.Cl. H02M 3/155
H02M 1/08

(21)Application number : 06-310732

(22)Date of filing : 14.12.1994

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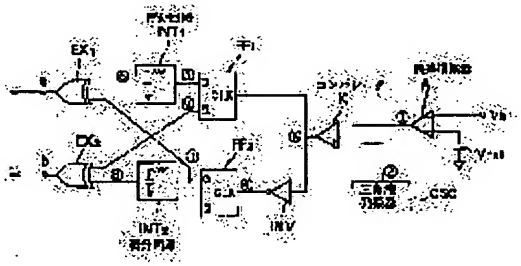
(54) CONTROL CIRCUIT FOR ZERO-VOLT SWITCH PULSE WIDTH MODULATION TYPE SWITCHING REGULATOR

(57)Abstract:

PURPOSE: To provide a control circuit which drives two switching elements contained in a zero-voltage switch pulse width modulation (ZVS-PWM) switching regulator.

CONSTITUTION: A pulse signal having the duty ratio corresponding to an error voltage and fixed frequency is generated by means of an error amplifier A which detects an error from a reference voltage Vref, triangular wave oscillator OSC, and comparator K. An inverter INV, flip flops FF1 and FF2, integration circuits INT1 and INT2, and exclusive OR circuits EX1 and EX2 generate the drive signals of two switching elements Q1 and Q1 based on the pulse signal. By using such a circuit configuration, the switching elements Q1 and Q2 are alternately turned on with a fixed dead time in between.



LEGAL STATUS

[Date of request for examination] 14.12.1994

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or

application converted registration]	
[Date of final disposal for application]	
[Patent number]	2677215
[Date of registration]	25.07.1997
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	25.07.2000

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平8－168239

(43)公開日　平成８年(1996)６月25日

(51)Int.Cl.⁶		識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０２Ｍ	3/155		Ｑ		
	1/08	３３１	Ｚ		

審査請求　有　請求項の数３　ＯＬ　（全５頁）

(21)出願番号　特願平6－310732

(22)出願日　平成６年(1994)12月14日

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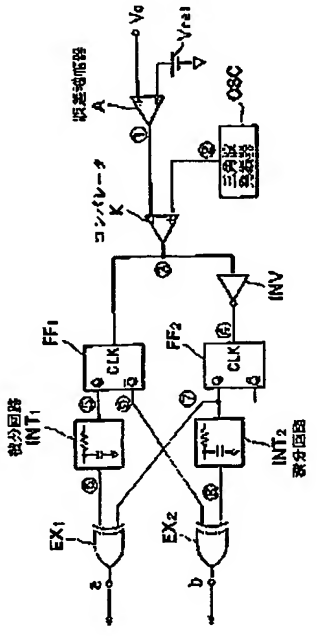
(54)【発明の名称】　ゼロボルトスイッチパルス幅変調型スイッチングレギュレータの制御回路

(57)【要約】
【目的】ゼロボルトスイッチパルス幅変調（ＺＶＳ－ＰＷＭ）型のスイッチングレギュレータに含まれる２つのスイッチ素子Q_1,Q_2を駆動する制御回路を提供する。
【構成】基準電圧V_{ref}との誤差を検出する誤差増幅器Ａと、三角波発振器ＯＳＣと、コンパレータＫとにより、誤差電圧に応じたデューティ比を有する一定周波数のパルス信号を生成する。このパルス信号に基づき、インバータＩＮＶ、フリップフロップFF_1,FF_2、積分回路INT_1,INT_2及び排他的論理和回路EX_1,EX_2とによって、２つのスイッチ素子Q_1,Q_2のそれぞれの駆動信号を生成する。この回路構成により、一定のデッドタイムをはさんで両方のスイッチ素子が交互にオン状態となる。



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【特許請求の範囲】

【請求項1】　ゼロボルトスイッチパルス幅変調型のスイッチングレギュレータの制御に使用される制御回路であって、

前記スイッチングレギュレータの出力電圧信号を入力とし前記出力電圧信号と基準電圧との誤差を検出する誤差増幅器と、前記誤差の大きさに応じたデューティ比を有する一定周波数のパルス信号を生成する信号生成回路と、前記信号生成回路の出力を反転するインバータと、前記信号生成回路の出力を入力とする第1のフリップフロップと、前記インバータの出力を入力とする第2のフリップフロップと、前記第1のフリップフロップの非反転出力を所定時間遅延させる第1の遅延回路と、前記第2のフリップフロップの非反転出力を前記所定時間遅延させる第2の遅延回路と、前記第1の遅延回路の出力と前記第2のフリップフロップの非反転出力とを入力とする第1の排他的論理和回路と、前記第2の遅延回路の出力と前記第1のフリップフロップの反転出力とを入力とする第2の排他的論理和回路とを有し、

前記各排他的論理和回路の出力が前記スイッチングレギュレータの各スイッチ素子のオン／オフ制御に使用されるゼロボルトスイッチパルス幅変調型スイッチングレギュレータの制御回路。

【請求項2】　前記信号生成回路が、一定周波数の三角波信号を発生する三角波発振器と、前記誤差増幅器の出力と前記三角波信号を比較してその結果を出力するコンパレータとによって構成された、請求項1に記載のゼロボルトスイッチパルス幅変調型スイッチングレギュレータの制御回路。

【請求項3】　同一の時定数を有する積分回路によって前記各遅延回路が構成され、前記各排他的論理和回路の入力のスレッショホルド電圧が同一である請求項1または2に記載のゼロボルトスイッチパルス幅変調型スイッチングレギュレータの制御回路。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、スイッチングレギュレータの制御回路に関し、特にゼロボルトスイッチング（ZVS）パルス幅変調（PWM）型のスイッチングレギュレータの制御回路に関する。

【0002】

【従来の技術】スイッチングレギュレータは、小型、高効率の電源として広く使用されており、各種の回路構成のものが実用化されている。スイッチングレギュレータでは、一般的に、パルス幅変調（PWM：Pulse Width Modulation）によって出力電圧の制御が行なわれている。PWM型のスイッチングレギュレータにおいてスイッチングノイズを低減するとともにさらなる電力変換効率の向上を実現する新しい技術として、ゼロボルトスイッチング（ZVS：Zero Volt Switching）が提唱されている（例えば、原田耕介、二宮保、顧文健、共著：「スイッチングコンバータの基礎」：コロナ社）。

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【0003】図3(a)は、ゼロボルトスイッチングパルス幅変調（以下、ZVS－PWMと称する）型のスイッチングレギュレータの基本回路図である。従来の降圧型のスイッチングレギュレータ回路における転流ダイオードを第2のスイッチ素子に取り替えるとともに、各スイッチ素子に並列にそれぞれコンデンサを接続した構成となっている。

【0004】すなわち、共通接地点と入力端子T_1との間に入力電源Eが接続されるものとして、入力端子T_1と共通接地点との間に、典型的にはパワーMOSトランジスタからなる第1及び第2のスイッチ素子Q_1,Q_2が直列に接続されており、各スイッチ素子Q_1,Q_2にはそれぞれコンデンサC_1,C_2が並列に接続されている。各スイッチ素子Q_1,Q_2は、それぞれのゲート端子G_1,G_2に印加される電圧でオン／オフの制御がなされるものである。スイッチ素子Q_1とスイッチ素子Q_2との接続点にチョークコイルLの一端が接続され、このチョークコイルLの他端は出力端子T_2に接続されている。出力端子T_2と共通接地点との間にはコンデンサC_3が設けられている。ここで出力端子T_2の電圧を出力電圧V_oとする。負荷抵抗Rは、端子T_2と共通接地点との間に接続される。

【0005】各スイッチ素子Q_1,Q_2の動作タイミングが図3(b)に示されている。ZVS－PWM型スイッチングレギュレータでは、スイッチ素子Q_1,Q_2を交互にオンさせるのであるが、その際、両方のスイッチ素子Q_1,Q_2がともにオフ状態となる期間（デッドタイムt_d）を設けて各スイッチ素子Q_1,Q_2でのゼロボルトスイッチングが実現できるようにし、これにより、スイッチングノイズを低減させるとともに電力変換効率を向上させている。第1のスイッチ素子Q_1のオン時間をt_1、第2のスイッチ素子Q_2のオフ時間をt_2、繰り返し周期をt_sとすると、デッドタイムt_dは、$t_s = t_1 + 2 \times t_d$を満足する一定時間である。また、第1のスイッチ素子Q_1のデューティ比D_1は、$D_1 = t_1 / t_s$であって、t_sを一定に保ちつつこのデューティ比D_1を変化させることにより、出力電圧V_oの制御が行なわれる。

【0006】

【発明が解決しようとする課題】ZVS－PWM型のスイッチングレギュレータについてはその基本回路構成は知られているものの、各スイッチ素子を適切に駆動するための実用的な制御回路はこれまで実現されておらず、このため、ZVS－PWM型スイッチングレギュレータ自体も実用化されていなかった。

【0007】本発明の目的は、ZVS－PWM型スイッチングレギュレータの制御回路であって、高精度かつ簡潔な回路を提供することにある。

【0008】

【課題を解決するための手段】本発明のゼロボルトスイッチパルス幅変調型スイッチングレギュレータの制御回路は、ゼロボルトスイッチパルス幅変調型のスイッチングレギュレータの制御に使用される制御回路であって、前記スイッチングレギュレータの出力電圧信号を入力とし前記出力電圧信号と基準電圧との誤差を検出する誤差増幅器と、前記誤差の大きさに応じたデューティ比を有する一定周波数のパルス信号を生成する信号生成回路と、前記信号生成回路の出力を反転するインバータと、前記信号生成回路の出力を入力とする第1のフリップフロップと、前記インバータの出力を入力とする第2のフリップフロップと、前記第1のフリップフロップの非反転出力を所定時間遅延させる第1の遅延回路と、前記第2のフリップフロップの非反転出力を前記所定時間遅延させる第2の遅延回路と、前記第1の遅延回路の出力と前記第2のフリップフロップの非反転出力とを入力とする第1の排他的論理和回路と、前記第2の遅延回路の出力と前記第1のフリップフロップの反転出力とを入力とする第2の排他的論理和回路とを有し、前記各排他的論理和回路の出力が前記スイッチングレギュレータの各スイッチ素子のオン／オフ制御に使用される。

【0009】本発明において、信号生成回路は、一定周波数の三角波信号を発生する三角波発振器と、誤差増幅器の出力と三角波信号を比較してその結果を出力するコンパレータとによって構成することができる。また、同一の時定数を有する積分回路によって各遅延回路を構成し、各排他的論理和回路の入力のスレッショホルド電圧が同一であるようにすることができる。

【0010】

【作用】フリップフロップと遅延回路と排他的論理和回路を2個ずつ使用して、デッドタイムを有する適切な出力が得られるようにしたので、ZVS－PWM型スイッチングレギュレータのための高精度の制御回路を簡潔な構成で実現できる。

【0011】

【実施例】次に、本発明の実施例について図面を参照して説明する。図1は本発明の一実施例のZVS－PWM型スイッチングレギュレータの制御回路の構成を示すブロック図であり、図2は図1の制御回路における各点の電圧の変化を示すタイミングチャートである。この制御回路は、図3(a)に基本回路図を示すZVS－PWM型スイッチングレギュレータの制御に好ましく使用されるものであって、スイッチングレギュレータの出力電圧V_oを入力とし、各スイッチ素子Q_1,Q_2の駆動信号を出力する。この駆動信号に基づき、不図示の駆動回路によって各スイッチ素子Q_1,Q_2のオン／オフ制御が行なわれる。

【0012】基準電圧V_{ref}とスイッチングレギュレータの出力電圧V_oとを入力とし、これらの間の誤差を検出して増幅する誤差増幅器Aが設けられている。また、一定の周波数で三角波を発振する三角波発振器OSCが設けられている。これら誤差増幅器Aの出力と三角波発振器OSCの出力は、コンパレータKに入力して相互に比較されるようになっている。さらにこの制御回路には、コンパレータKの出力が入力してこれを反転するインバータINVと、コンパレータKの出力をクロック入力とする第1のT型フリップフロップFF_1と、インバータINVの出力をクロック入力とする第2のT型フリップフロップFF_2と、第1のフリップフロップのFF_1の非反転出力Qが入力する第1の積分回路INT_1と、第2のフリップフロップFF_2の非反転出力Qが入力する第2の積分回路INT_2と、第1の積分回路INT_1の出力及び第2のフリップフロップの非反転出力Qを入力とする第1の排他的論理和回路EX_1と、第2の積分回路INT_2の出力及び第1のフリップフロップFF_1の反転出力

【0013】

【外1】

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を入力とする第2の排他的論理和回路EX_2とを有する。第1の排他的論理和回路EX_1からの出力信号は、端子aを介して、スイッチングレギュレータの第1のスイッチ素子Q_1（図3参照）の駆動信号となり、同様に第2の排他的論理和回路EX_2からの出力信号は、端子bを介して、スイッチ素子Q_2の駆動信号となる。

【0014】積分回路INT_1,INT_2は、入力信号を所定の同一時間だけ遅延させるためのものであり、抵抗とコンデンサからなるCR型のものであって、同一の時定数を有する。また排他的論理和回路EX_1,EX_2は、入力電圧特性に関し、同一のスレッショホルド電圧を有する。

【0015】次に、この制御回路の動作を説明する。誤差増幅器Aによりスイッチングレギュレータの出力電圧V_oと基準電圧V_{ref}との誤差が増幅され（図2の①参照）、また、三角波発振器OSCは一定周波数の三角波を出力する（図2の②参照）。以下の説明から明らかなように、三角波の周期が繰り返し周期t_sとなる。コンパレータKは、誤差増幅器Aの出力（図2の①）と三角波発振器OSCの出力（図2の②）を比較し、図2の③に示されるように、三角波の方の電圧が上回っている期間、論理値"1"を出力し、その他の期間は論理値"0"を出力する。したがって、コンパレータKの出力信号のデューティ比は、誤差増幅器Aで検出された誤差の大きさに対応することになる。

【0016】コンパレータKの出力は、第1のT型フリップフロップFF_1のクロック端子CLKに入力するとともに、インバータINVによって反転されて（図2の④参照）、第2のT型フリップフロップFF_2のクロック端子CLKに入力する。各フリップフロップFF_1,FF_2がポジティブエッジトリガであるとすると、第1の

フリップフロップＦＦ₁の非反転出力Ｑおよび反転出力

【００１７】

【外２】

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は、それぞれ、図２の⑤及び⑥で示されるようになり、第２のフリップフロップＦＦ₂の非反転出力Ｑは図２の⑦で示されるようになる。第１のフリップフロップＦＦ₁の出力と第２のフリップフロップＦＦ₂の出力とは、コンパレータＫの出力パルスの幅だけ、すなわち、上述の誤差の大きさに応じて、時間的にずれている。

【００１８】積分回路ＩＮＴ₁，ＩＮＴ₂では、フリップフロップＦＦ₁，ＦＦ₂の非反転出力Ｑが、そのＣＲの時定数に応じて積分される。積分回路ＩＮＴ₁，ＩＮＴ₂の出力が、図２の⑧と⑨にそれぞれ示されている。第１の排他的論理和回路ＥＸ₁は、第１の積分回路ＩＮＴ₁の出力と第２のフリップフロップＦＦ₂の非反転出力Ｑとの排他的論理和を求めて出力する（図２のａ参照）。すなわち、コンパレータＫの出力と同様であるが、積分回路ＩＮＴ₁の時定数と排他的論理和回路ＥＸ₁の入力のスレッショホルド電圧で定まる所定の時間だけ、パルスの立上りの時点が遅延している出力が得られる。ここではこの所定の時間がＺＶＳ－ＰＷＭ型スイッチングレギュレータのデッドタイムt_dと一致するように、時定数やスレッショホルド電圧を定めるようにしておく。同様に、第２の排他的論理和回路ＥＸ₂は、第２の積分回路ＩＮＴ₂の出力と第１のフリップフロップＦＦ₁の反転出力との排他的論理和を求めて出力する（図２のｂ参照）。したがって、第２の排他的論理和回路ＥＸ₂からは、インバータＩＮＶの出力と同様であるが、パルスの立上りがデッドタイムt_dだけ遅れた出力が得られる。

【００１９】上述したように、デッドタイムt_dは、積分回路ＩＮＴ₁，ＩＮＴ₂の時定数と排他的論理和回路ＥＸ₁，ＥＸ₂のスレッショホルド電圧によって決定するので、一定である。繰り返し時間t_sは三角波発振器ＯＳＣの発振周波数で定まるので一定であり、端子ａが"１"である時間t_aはスイッチングレギュレータの出力電圧V_oと基準電圧V_{ref}との誤差に応じて変化することになる。したがって、$t_a = t_s + 2 \times t_d$が常に成立する。

ＺＶＳ－ＰＷＭ型スイッチングレギュレータの各素子の定数、入力電圧及び所望の出力電圧に応じて繰り返し周期t_sやデッドタイムt_dを定め、また、誤差増幅器Ａのゲインなどを適切に設定し、端子ａ，ｂからの出力によってスイッチ素子Q_1，Q_2がそれぞれオン／オフ制御されるようにしておくことにより、この制御回路によってＺＶＳ－ＰＷＭ型スイッチングレギュレータを適切に制御することができることになる。

【００２０】

【発明の効果】以上説明したように本発明は、フリップフロップと遅延回路と排他的論理和回路などを使用する簡潔な回路構成で、ＺＶＳ－ＰＷＭ型スイッチングレギュレータのための高精度の制御回路を構成でき、ＺＶＳ－ＰＷＭ型スイッチングレギュレータが容易に実現できるようになるという効果がある。

【図面の簡単な説明】

【図１】本発明の一実施例のＺＶＳ－ＰＷＭ型スイッチングレギュレータの制御回路の構成を示すブロック図である。

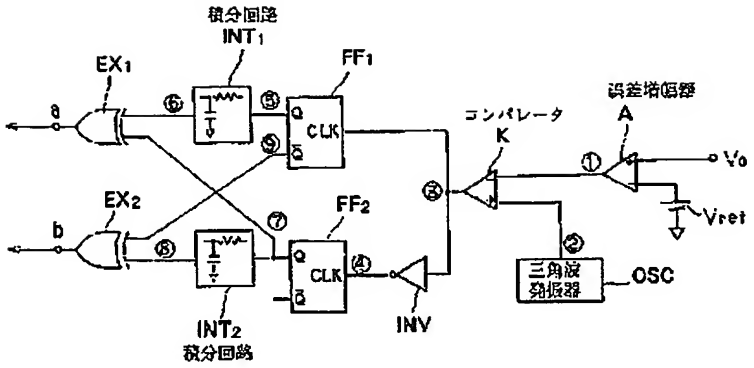
【図２】図１の制御回路のフローチャートである。

【図３】(a)はＺＶＳ－ＰＷＭ型スイッチングレギュレータの基本回路図、(b)は各スイッチ素子に対する駆動信号を示すタイミングチャートである。

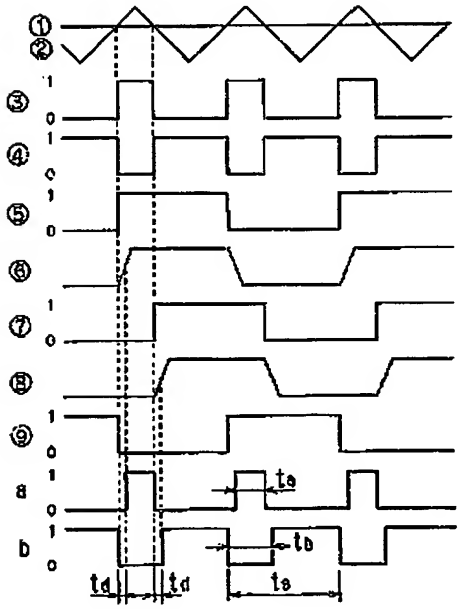
【符号の説明】

Ａ　誤差増幅器
Ｅ　入力電源
EX_1，EX_2　排他的論理和回路
FF_1，FF_2　フリップフロップ
G_1，G_2　ゲート端子
Ｋ　コンパレータ
ＩＮＶ　インバータ
INT_1，INT_2　積分回路
ＯＳＣ　三角波発振器
Q_1，Q_2　スイッチ素子
T_1，T_2　端子
Ｒ　負荷抵抗
V_o　出力電圧
V_{ref}　基準電圧

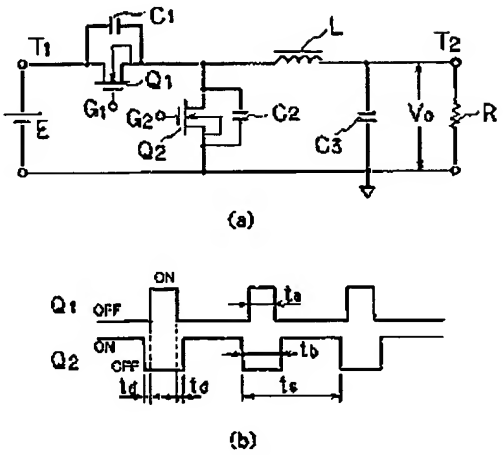
【図1】


積分回路
INT1
EX1
FF1
a
CLK
コンパレータ
K
誤差増幅器
A
Vo
EX2
FF2
b
CLK
Vref
三角波
発振器
OSC
INV
INT2
積分回路

【図2】


①
②
③
④
⑤
⑥
⑦
⑧
⑨
a
b
ta
tb
td
td
ta

【図3】


C1
L
T1
T2
Q1
G1
G2
C2
E
Q2
C3
Vo
R
(a)
Q1
ON
OFF
ta
Q2
ON
OFF
tb
td
td
ta
(b)

Japanese Patent Application Publication No. 08-168239

CLAIMS

[Claim(s)]

[Claim 1] It is the control circuit used for control of a switching regulator of a zero bolt switch Pulse-Density-Modulation mold. Error amplifier which considers an output voltage signal of said switching regulator as an input, and detects an error of said output voltage signal and reference voltage, A signal generation circuit which generates a pulse signal of constant frequency which has a duty ratio according to magnitude of said error, An inverter which reverses an output of said signal generation circuit, and the 1st flip-flop which considers an output of said signal generation circuit as an input, The 2nd flip-flop which considers an output of said inverter as an input, and the 1st delay circuit which carries out predetermined time delay of the noninverting output of said 1st flip-flop, A noninverting output of said 2nd flip-flop Said 2nd delay circuit which carries out predetermined time delay, The 1st exclusive "or" circuit which considers an output of said 1st delay circuit, and a noninverting output of said 2nd flip-flop as an input, It has the 2nd exclusive "or" circuit which considers an output of said 2nd delay circuit, and a reversal output of said 1st flip-flop as an input. A control circuit of a zero bolt switch Pulse-Density-Modulation mold switching regulator where an output of each of said exclusive "or" circuit is used for ON / off control of each switching device of said switching regulator.

[Claim 2] A control circuit of a zero bolt switch Pulse-Density-Modulation mold switching regulator according to claim 1 constituted by comparator which said signal generation circuit compares an output and said chopping sea signal of a chopping sea oscillator which generates a chopping sea signal of constant frequency, and said error amplifier, and outputs the result.

[Claim 3] Said each delay circuit is constituted by integrating circuit which has the same time constant, and it is the control circuit of a zero bolt switch Pulse-Density-Modulation mold switching regulator according to claim 1 or 2 with same SURESSHOHORUDO voltage of an input of each of said exclusive "or" circuit.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to the control circuit of the switching regulator of a zero bolt switching (ZVS) Pulse-Density-Modulation (PWM) mold about the control circuit of a switching regulator.
[0002]
[Description of the Prior Art] It is widely used as a power supply small [a switching regulator] and efficient, and the thing of various kinds of circuitry is put in practical use. Generally in the switching regulator, control of output voltage is performed by Pulse Density Modulation (PWM;Pulse Width Modulation). While reducing a switching noise in the switching regulator of an PWM mold, as new technology of realizing improvement in the further power conversion effectiveness, zero bolt switching (ZVS;Zero Volt Switching) is advocated (for example, Kosuke Harada, 2 Miyayasu, ******, collaboration : "the base of a switching converter": Corona Publishing).
[0003] Drawing 3 (a) is the basic circuit diagram of the switching regulator of a zero bolt switching Pulse-Density-Modulation (ZVS-PWM is called hereafter) mold. While exchanging the commutation diode in the switching regulator circuit of the conventional pressure-lowering mold to the 2nd switching device, it is each switching device with the configuration of having connected the capacitor to juxtaposition, respectively.
[0004] That is, the 1st and 2nd switching devices Q1 and Q2 which consist of a power MOS transistor typically are connected to the serial between the input terminal T1 and the common-electrical-ground point as that by which input power E is connected between a common-electrical-ground point and an input terminal T1, and capacitors C1 and C2 are connected to each switching devices Q1 and Q2 at juxtaposition, respectively. ON / off control is made on the voltage on which each switching devices Q1 and Q2 are impressed to each gate terminal G1 and G2. The end of a choke coil L is connected at the node of a switching device Q1 and a switching device Q2, and the other end of this choke coil L is connected to the output terminal T2. The capacitor C3 is formed between the output terminal T2 and the common-electrical-ground point. Let voltage of an output terminal T2 be output voltage Vo here. Load resistance R is connected between a terminal T2 and a common-electrical-ground point.
[0005] The timing of each switching devices Q1 and Q2 of operation is shown in drawing 3 (b). In the ZVS-PWM mold switching regulator, although switching devices Q1 and Q2 are made to turn on by turns, in that case, establish the period (dead time td) when both both switching devices Q1 and Q2 will be in an OFF state, and it enables it to realize zero bolt switching by each switching devices Q1 and Q2, and while reducing a switching noise, thereby, power conversion effectiveness is raised. When ta and OFF time amount of the 2nd switching device Q2 are set to tb and a repeat period is set to ts for the ON time amount of the 1st switching device Q1, a dead time td is fixed time amount with which are satisfied of tb=ta+2xtd. Moreover, the duty ratio Da of the 1st switching device Q1 is Da=ta/ts, and control of output voltage Vo is performed by changing this duty ratio Da, keeping td constant.
[0006]
[Problem(s) to be Solved by the Invention] Although that basic circuitry was known about the switching regulator of a ZVS-PWM mold, the practical control circuit for driving each switching

device appropriately was not realized until now, and, for this reason, the ZVS-PWM mold switching regulator itself was not put in practical use.
[0007] The object of this invention is the control circuit of a ZVS-PWM mold switching regulator, and is to offer high degree of accuracy and a brief circuit.
[0008]
[Means for Solving the Problem] A control circuit of a zero bolt switch Pulse-Density-Modulation mold switching regulator of this invention It is the control circuit used for control of a switching regulator of a zero bolt switch Pulse-Density-Modulation mold. Error amplifier which considers an output voltage signal of said switching regulator as an input, and detects an error of said output voltage signal and reference voltage, A signal generation circuit which generates a pulse signal of constant frequency which has a duty ratio according to magnitude of said error, An inverter which reverses an output of said signal generation circuit, and the 1st flip-flop which considers an output of said signal generation circuit as an input, The 2nd flip-flop which considers an output of said inverter as an input, and the 1st delay circuit which carries out predetermined time delay of the noninverting output of said 1st flip-flop, A noninverting output of said 2nd flip-flop Said 2nd delay circuit which carries out predetermined time delay, The 1st exclusive "or" circuit which considers an output of said 1st delay circuit, and a noninverting output of said 2nd flip-flop as an input, It has the 2nd exclusive "or" circuit which considers an output of said 2nd delay circuit, and a reversal output of said 1st flip-flop as an input, and an output of each of said exclusive "or" circuit is used for ON / off control of each switching device of said switching regulator.
[0009] In this invention, a chopping sea oscillator which generates a chopping sea signal of constant frequency, and a comparator which compares an output and a chopping sea signal of error amplifier, and outputs the result can constitute a signal generation circuit. moreover, an integrating circuit which has the same time constant -- each delay circuit -- constituting -- SURESSHOHORUDO voltage of an input of each exclusive "or" circuit -- the same -- making .
[0010]
[Function] It uses a flip-flop, a delay circuit, and two exclusive "or" circuits at a time, and since the suitable output which has a dead time was obtained, the control circuit of the high degree of accuracy for a ZVS-PWM mold switching regulator is realizable with a brief configuration.
[0011]
[Example] Next, the example of this invention is explained with reference to a drawing. Drawing 1 is the block diagram showing the configuration of the control circuit of the ZVS-PWM mold switching regulator of one example of this invention, and drawing 2 is a timing chart which shows change of the voltage of each point in the control circuit of drawing 1 . This control circuit is preferably used for control of the ZVS-PWM mold switching regulator which shows a basic circuit diagram to drawing 3 (a), considers output voltage Vo of a switching regulator as an input, and outputs the driving signal of each switching devices Q1 and Q2. Based on this driving signal, ON / off control of each switching devices Q1 and Q2 are performed by the non-illustrated actuation circuit.
[0012] Reference voltage Vref and output voltage Vo of a switching regulator are considered as an input, and the error amplifier A which detects and amplifies the error between these is formed. Moreover, the chopping sea oscillator OSC which oscillates a chopping sea on fixed frequency is formed. The output of these error amplifier A and the output of the chopping sea oscillator OSC are inputted into Comparator K, and are measured mutually. The inverter INV which the output of Comparator K inputs into this control circuit, and furthermore reverses this to it, 1st T mold

flip-flop FF 1 which makes the output of Comparator K clocked into 2nd T mold flip-flop FF 2 which makes the output of Inverter INV clocked into The 1st integrating circuit INT 1 which the noninverting output Q of FF1 of the 1st flip-flop inputs The 2nd integrating circuit INT 2 which the noninverting output Q of the 2nd flip-flop FF 2 inputs The output of the 1st exclusive "or" circuit EX1 which considers the output of the 1st integrating circuit INT 1, and the noninverting output Q of the 2nd flip-flop as an input, and the 2nd integrating circuit INT 2, and the reversal output of the 1st flip-flop FF 1 [0013]
[External Character 1]

It has the 2nd exclusive "or" circuit EX2 considered as an input. The output signal from the 1st exclusive "or" circuit EX1 turns into a driving signal of the 1st switching device Q1 (refer to drawing 3) of a switching regulator through Terminal a, and the output signal from the 2nd exclusive "or" circuit EX2 turns into a driving signal of a switching device Q2 through Terminal b similarly.
[0014] Integrating circuits INT1 and INT2 are only for the same predetermined time amount to delay an input signal, are the things of CR mold which consists of resistance and a capacitor, and have the same time constant. Moreover, exclusive "or" circuits EX1 and EX2 have the same SURESSHOHORUDO voltage about an input voltage property.
[0015] Next, actuation of this control circuit is explained. The error of the output voltage Vo of a switching regulator and reference voltage Vref is amplified by the error amplifier A (refer to ** of drawing 2), and the chopping sea oscillator OSC outputs the chopping sea of constant frequency (refer to ** of drawing 2). The period of a chopping sea turns into the repeat period ts so that clearly from the following explanation. As Comparator K measures the output (** of drawing 2) of the error amplifier A, and the output (** of drawing 2) of the chopping sea oscillator OSC and it is shown in ** of drawing 2 , the period which the voltage in the direction of a chopping sea has exceeded, and logical-value"1" are outputted, and other periods output logical-value"0." Therefore, the duty ratio of the output signal of Comparator K will be equivalent to the magnitude of the error detected with the error amplifier A.
[0016] It is reversed with Inverter INV (refer to ** of drawing 2), and the output of Comparator K is inputted into the clock terminal CLK of 2nd T mold flip-flop FF 2 while inputting it into the clock terminal CLK of 1st T mold flip-flop FF 1. Supposing each flip-flops FF1 and FF2 are positive edge triggers, it is the noninverting output Q and reversal output [0017] of the 1st flip-flop FF 1.
[External Character 2]

It comes to be shown by **, ** which is drawing 2 , and **, respectively, and the noninverting output Q of the 2nd flip-flop FF 2 comes to be shown by ** of drawing 2 . According to the magnitude of the error above-mentioned [the output of the 1st flip-flop FF 1 and the output of the 2nd flip-flop FF 2 / the width of face of the output pulse of Comparator K], it is shifted in time.
[0018] The noninverting output Q of flip-flops FF1 and FF2 integrates integrating circuits INT1 and INT2 according to the time constant of the CR. The output of integrating circuits INT1 and INT2 is shown in ** and ** of drawing 2 , respectively. The 1st exclusive "or" circuit EX1 is outputted in quest of the exclusive OR of the output of the 1st integrating circuit INT 1, and the

noninverting output Q of the 2nd flip-flop FF 2 (refer to a of drawing 2). That is, although it is the same as that of the output of Comparator K, only the time constant of an integrating circuit INT 1 and the predetermined time amount which becomes settled on the SURESSHOHORUDO voltage of the input of an exclusive "or" circuit EX1 are acquired for the output by which the event of the standup of a pulse is delayed. Here, a time constant and SURESSHOHORUDO voltage are defined so that this predetermined time amount may be in agreement with the dead time td of a ZVS-PWM mold switching regulator. Similarly, the 2nd exclusive "or" circuit EX2 is outputted in quest of the exclusive OR of the output of the 2nd integrating circuit INT 2, and the reversal output of the 1st flip-flop FF 1 (refer to b of drawing 2). Therefore, although it is the same as that of the output of Inverter INV, the output only the dead time td was behind [output] in the standup of a pulse is obtained from the 2nd exclusive "or" circuit EX2.

[0019] As mentioned above, since the time constant of integrating circuits INT1 and INT2 and the SURESSHOHORUDO voltage of exclusive "or" circuits EX1 and EX2 determine a dead time td, it is fixed. The time amount ta whose terminal a it is fixed since repetition time ts becomes settled on the oscillation frequency of the chopping sea oscillator OSC, and is "1" will change according to the error of the output voltage Vo of a switching regulator, and reference voltage Vref. Therefore, tb=ta+2xtd is always materialized. When the repeat period ts and a dead time td are defined according to the constant of each element of a ZVS-PWM mold switching regulator, input voltage, and desired output voltage, and the gain of the error amplifier A etc. is set up appropriately and ON/OFF control of the switching devices Q1 and Q2 is made to be carried out by the output from Terminals a and b, respectively, a ZVS-PWM mold switching regulator can be appropriately controlled by this control circuit.

[0020]

[Effect of the Invention] As explained above, this invention is brief circuitry which uses a flip-flop, a delay circuit, an exclusive "or" circuit, etc., can constitute the control circuit of the high degree of accuracy for a ZVS-PWM mold switching regulator, and is effective in the ability of a ZVS-PWM mold switching regulator to realize now easily.

TECHNICAL FIELD

[Industrial Application] Especially this invention relates to the control circuit of the switching regulator of a zero bolt switching (ZVS) Pulse-Density-Modulation (PWM) mold about the control circuit of a switching regulator.

PRIOR ART

[Description of the Prior Art] It is widely used as a power supply small [a switching regulator] and efficient, and the thing of various kinds of circuitry is put in practical use. Generally in the switching regulator, control of output voltage is performed by Pulse Density Modulation (PWM;Pulse Width Modulation). While reducing a switching noise in the switching regulator of an PWM mold, as new technology of realizing improvement in the further power conversion effectiveness, zero bolt switching (ZVS;Zero Volt Switching) is advocated (for example, Kosuke Harada, 2 Miyayasu, ******, collaboration : "the base of a switching converter": Corona Publishing).

[0003] Drawing 3 (a) is the basic circuit diagram of the switching regulator of a zero bolt switching Pulse-Density-Modulation (ZVS-PWM is called hereafter) mold. While exchanging the commutation diode in the switching regulator circuit of the conventional pressure-lowering mold to the 2nd switching device, it is each switching device with the configuration of having connected the capacitor to juxtaposition, respectively.

[0004] That is, the 1st and 2nd switching devices Q1 and Q2 which consist of a power MOS transistor typically are connected to the serial between the input terminal T1 and the common-electrical-ground point as that by which input power E is connected between a common-electrical-ground point and an input terminal T1, and capacitors C1 and C2 are connected to each switching devices Q1 and Q2 at juxtaposition, respectively. ON / off control is made on the voltage on which each switching devices Q1 and Q2 are impressed to each gate terminal G1 and G2. The end of a choke coil L is connected at the node of a switching device Q1 and a switching device Q2, and the other end of this choke coil L is connected to the output terminal T2. The capacitor C3 is formed between the output terminal T2 and the common-electrical-ground point. Let voltage of an output terminal T2 be output voltage Vo here. Load resistance R is connected between a terminal T2 and a common-electrical-ground point.

[0005] The timing of each switching devices Q1 and Q2 of operation is shown in drawing 3 (b). In the ZVS-PWM mold switching regulator, although switching devices Q1 and Q2 are made to turn on by turns, in that case, establish the period (dead time td) when both both switching devices Q1 and Q2 will be in an OFF state, and it enables it to realize zero bolt switching by each switching devices Q1 and Q2, and while reducing a switching noise, thereby, power conversion effectiveness is raised. When ta and OFF time amount of the 2nd switching device Q2 are set to tb and a repeat period is set to ts for the ON time amount of the 1st switching device Q1, a dead time td is fixed time amount with which are satisfied of tb=ta+2xtd. Moreover, the duty ratio Da of the 1st switching device Q1 is Da=ta/ts, and control of output voltage Vo is performed by changing this duty ratio Da, keeping td constant.

EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, this invention is brief circuitry which uses a flip-flop, a delay circuit, an exclusive "or" circuit, etc., can constitute the control circuit of the high degree of accuracy for a ZVS-PWM mold switching regulator, and is effective in the ability of a ZVS-PWM mold switching regulator to realize now easily.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Although that basic circuitry was known about the switching regulator of a ZVS-PWM mold, the practical control circuit for driving each switching device appropriately was not realized until now, and, for this reason, the ZVS-PWM mold switching regulator itself was not put in practical use.
[0007] The object of this invention is the control circuit of a ZVS-PWM mold switching regulator, and is to offer high degree of accuracy and a brief circuit.
[0008]

MEANS

[Means for Solving the Problem] A control circuit of a zero bolt switch Pulse-Density-Modulation mold switching regulator of this invention It is the control circuit used for control of a switching regulator of a zero bolt switch Pulse-Density-Modulation mold. Error amplifier which considers an output voltage signal of said switching regulator as an input, and detects an error of said output voltage signal and reference voltage, A signal generation circuit which generates a pulse signal of constant frequency which has a duty ratio according to magnitude of said error, An inverter which reverses an output of said signal generation circuit, and the 1st flip-flop which considers an output of said signal generation circuit as an input, The 2nd flip-flop which considers an output of said inverter as an input, and the 1st delay circuit which carries out predetermined time delay of the noninverting output of said 1st flip-flop, A noninverting output of said 2nd flip-flop Said 2nd delay circuit which carries out predetermined time delay, The 1st exclusive "or" circuit which considers an output of said 1st delay circuit, and a noninverting output of said 2nd flip-flop as an input, It has the 2nd exclusive "or" circuit which considers an output of said 2nd delay circuit, and a reversal output of said 1st flip-flop as an input, and an output of each of said exclusive "or" circuit is used for ON / off control of each switching device of said switching regulator.

[0009] In this invention, a chopping sea oscillator which generates a chopping sea signal of constant frequency, and a comparator which compares an output and a chopping sea signal of error amplifier, and outputs the result can constitute a signal generation circuit. moreover, an integrating circuit which has the same time constant -- each delay circuit -- constituting -- SURESSHOHORUDO voltage of an input of each exclusive "or" circuit -- the same -- making .

OPERATION

[Function] It uses a flip-flop, a delay circuit, and two exclusive "or" circuits at a time, and since the suitable output which has a dead time was obtained, the control circuit of the high degree of accuracy for a ZVS-PWM mold switching regulator is realizable with a brief configuration.

EXAMPLE

[Example] Next, the example of this invention is explained with reference to a drawing. Drawing 1 is the block diagram showing the configuration of the control circuit of the ZVS-PWM mold switching regulator of one example of this invention, and drawing 2 is a timing chart which shows change of the voltage of each point in the control circuit of drawing 1 . This control circuit is preferably used for control of the ZVS-PWM mold switching regulator which shows a basic circuit diagram to drawing 3 (a), considers output voltage Vo of a switching regulator as an input, and outputs the driving signal of each switching devices Q1 and Q2. Based on this driving signal, ON / off control of each switching devices Q1 and Q2 are performed by the non-illustrated actuation circuit.

[0012] Reference voltage Vref and output voltage Vo of a switching regulator are considered as an input, and the error amplifier A which detects and amplifies the error between these is formed. Moreover, the chopping sea oscillator OSC which oscillates a chopping sea on fixed frequency is formed. The output of these error amplifier A and the output of the chopping sea oscillator OSC are inputted into Comparator K, and are measured mutually. The inverter INV which the output of Comparator K inputs into this control circuit, and furthermore reverses this to it, 1st T mold flip-flop FF 1 which makes the output of Comparator K clocked into 2nd T mold flip-flop FF 2 which makes the output of Inverter INV clocked into The 1st integrating circuit INT 1 which the noninverting output Q of FF1 of the 1st flip-flop inputs The 2nd integrating circuit INT 2 which the noninverting output Q of the 2nd flip-flop FF 2 inputs The output of the 1st exclusive "or" circuit EX1 which considers the output of the 1st integrating circuit INT 1, and the noninverting output Q of the 2nd flip-flop as an input, and the 2nd integrating circuit INT 2, and the reversal output of the 1st flip-flop FF 1 [0013]

[External Character 1]

It has the 2nd exclusive "or" circuit EX2 considered as an input. The output signal from the 1st exclusive "or" circuit EX1 turns into a driving signal of the 1st switching device Q1 (refer to drawing 3) of a switching regulator through Terminal a, and the output signal from the 2nd exclusive "or" circuit EX2 turns into a driving signal of a switching device Q2 through Terminal b similarly.

[0014] Integrating circuits INT1 and INT2 are only for the same predetermined time amount to delay an input signal, are the things of CR mold which consists of resistance and a capacitor, and have the same time constant. Moreover, exclusive "or" circuits EX1 and EX2 have the same SURESSHOHORUDO voltage about an input voltage property.

[0015] Next, actuation of this control circuit is explained. The error of the output voltage Vo of a switching regulator and reference voltage Vref is amplified by the error amplifier A (refer to ** of drawing 2), and the chopping sea oscillator OSC outputs the chopping sea of constant frequency (refer to ** of drawing 2). The period of a chopping sea turns into the repeat period ts so that clearly from the following explanation. As Comparator K measures the output (** of drawing 2) of the error amplifier A, and the output (** of drawing 2) of the chopping sea oscillator OSC and it is shown in ** of drawing 2 , the period which the voltage in the direction of a chopping sea has exceeded, and logical-value"1" are outputted, and other periods output logical-value"0." Therefore, the duty ratio of the output signal of Comparator K will be

equivalent to the magnitude of the error detected with the error amplifier A.
[0016] It is reversed with Inverter INV (refer to ** of drawing 2), and the output of Comparator K is inputted into the clock terminal CLK of 2nd T mold flip-flop FF 2 while inputting it into the clock terminal CLK of 1st T mold flip-flop FF 1. Supposing each flip-flops FF1 and FF2 are positive edge triggers, it is the noninverting output Q and reversal output [0017] of the 1st flip-flop FF 1.
[External Character 2]

It comes to be shown by **, ** which is drawing 2 , and **, respectively, and the noninverting output Q of the 2nd flip-flop FF 2 comes to be shown by ** of drawing 2 . According to the magnitude of the error above-mentioned [the output of the 1st flip-flop FF 1 and the output of the 2nd flip-flop FF 2 / the width of face of the output pulse of Comparator K], it is shifted in time.
[0018] The noninverting output Q of flip-flops FF1 and FF2 integrates integrating circuits INT1 and INT2 according to the time constant of the CR. The output of integrating circuits INT1 and INT2 is shown in ** and ** of drawing 2 , respectively. The 1st exclusive "or" circuit EX1 is outputted in quest of the exclusive OR of the output of the 1st integrating circuit INT 1, and the noninverting output Q of the 2nd flip-flop FF 2 (refer to a of drawing 2). That is, although it is the same as that of the output of Comparator K, only the time constant of an integrating circuit INT 1 and the predetermined time amount which becomes settled on the SURESSHOHORUDO voltage of the input of an exclusive "or" circuit EX1 are acquired for the output by which the event of the standup of a pulse is delayed. Here, a time constant and SURESSHOHORUDO voltage are defined so that this predetermined time amount may be in agreement with the dead time td of a ZVS-PWM mold switching regulator. Similarly, the 2nd exclusive "or" circuit EX2 is outputted in quest of the exclusive OR of the output of the 2nd integrating circuit INT 2, and the reversal output of the 1st flip-flop FF 1 (refer to b of drawing 2). Therefore, although it is the same as that of the output of Inverter INV, the output only the dead time td was behind [output] in the standup of a pulse is obtained from the 2nd exclusive "or" circuit EX2.
[0019] As mentioned above, since the time constant of integrating circuits INT1 and INT2 and the SURESSHOHORUDO voltage of exclusive "or" circuits EX1 and EX2 determine a dead time td, it is fixed. The time amount ta whose terminal a it is fixed since repetition time ts becomes settled on the oscillation frequency of the chopping sea oscillator OSC, and is "1" will change according to the error of the output voltage Vo of a switching regulator, and reference voltage Vref. Therefore, tb=ta+2xtd is always materialized. When the repeat period ts and a dead time td are defined according to the constant of each element of a ZVS-PWM mold switching regulator, input voltage, and desired output voltage, and the gain of the error amplifier A etc. is set up appropriately and ON/OFF control of the switching devices Q1 and Q2 is made to be carried out by the output from Terminals a and b, respectively, a ZVS-PWM mold switching regulator can be appropriately controlled by this control circuit.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the configuration of the control circuit of the ZVS-PWM mold switching regulator of one example of this invention.
[Drawing 2] It is the flow chart of the control circuit of drawing 1 .
[Drawing 3] It is the timing chart which shows a driving signal [as opposed to / as opposed to / in (a) / the basic circuit diagram of a ZVS-PWM mold switching regulator / each switching device in (b)].
[Description of Notations]
A Error amplifier
E Input power
EX1, EX2 Exclusive "or" circuit
FF1, FF2 Flip-flop
G1, G2 Gate terminal
K Comparator
INV Inverter
INT1, INT2 Integrating circuit
OSC Chopping sea oscillator
Q1, Q2 Switching device
T1, T2 Terminal
R Load resistance
Vo Output voltage
Vref Reference voltage